JAIN UNIVERSITY

Estd. u/s 3 of the UGC Act, 1956

School of Engineering and Technology

Department of Electronics & Communication Engineering

M.Tech Syllabus

In

Embedded System Design

2014-2015

Scheme of Teaching and Examination

Semester I

	Subject Code	Name of the Subject	Teaching/ Practical Hours per Week	Credits	Duration of the Exam	I.A. Marks	Exam Marks	Total
1	14MTES101	Embedded System Design	4	4	3	50	50	100
2	14MTES102	Advanced Microprocessors for Embedded System Design	4	4	3	50	50	100
3	14MTES103	Embedded Programming using C	4	4	3	50	50	100
4	14MTES104	Embedded Real Time Operating Systems	4	4	3	50	50	100
5	14MTES105	Automotive Electronics	4	4	3	50	50	100
6	14MTES116	**A**dvanced Microprocessor Lab	2	2	3	50	50	100
		Total		22		300	300	600

Semester II

	Subject Code	Name of the Subject	Teaching/ Practical Hours per Week	Credits	Duration of the Exam	I.A. Marks	Exam Marks	Total
1	14MTES201	DSP system & Architecture	4	4	3	50	50	100
2	14MTES202	VLSI Technology and Design	4	4	3	50	50	100
3	14MTES203	Engg. Approach to Digital Design	4	4	3	50	50	100
4	14MTES204	Embedded System Communication and networks	4	4	3	50	50	100
5	14MTES2XX	Elective 1	4	4	3	50	50	100
6	14MTES216	VLSI and Embedded System Design Lab	2	2	3	50	50	100
		Total		22		300	300	600

Elective 1

Subject Code	Name of the Subject
14MTES251	MEMS
14MTES252	Advanced Operating Systems
14MTES253	System On Chip Architecture
14MTES254	Wireless LAN's and PAN's

Semester III

	Subject Code	Name of the Subject	Teaching/ Practical Hours per Week	Credits	Duration of the Exam	I.A. Marks	Exam Marks	Total
1	14MTES301	Electronic Packaging	4	4	3	50	50	100
2	13MTES302	Model Based Development of Embedded system	4	4	3	50	50	100
3	13MTES3XX	Elective 2	4	4	--	50	50	100
4	13MTES301	Seminar/ Mini Project	--	2	--	50	--	50
5		Internship	--	2		50		50
		Total		16		250	150	400

Elective 2

Subject Code	Name of the Subject
14MTES331	Hardware and Software Co-Design
14MTES332	Embedded Computing
14MTES333	Advanced Computer Architecture
14MTES334	Network Security and Cryptography

Semester IV

Subject Code	Name of the Subject	Hours per week			Credits	Marks		
		Lecture	Tutorial	Practical		I.A. Marks	Exam Marks	Total
14MTES401	Project work and Dissertation	--	--	--	20	100	300+ 100(Viva)	500
	Total	--	--	--	20	100	400	500

SEMESTER-I

SEMESTER- I

Embedded System Design

Subject Code: 14MTES101 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

UNIT -I:

Introduction to Embedded Systems

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems. **12 Hours**

UNIT -II:

Typical Embedded System:

Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

12 Hours

UNIT -III:

Embedded Firmware:

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages. **12 Hours**

Part B

UNIT -IV:

RTOS Based Embedded System Design:

Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling. **12 Hours**

UNIT -V:

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS. **12 Hours**

TEXT BOOKS:

1. Shibu K.V "Introduction to Embedded Systems", Mc Graw Hill 4th Edition 2009
2. Raj Kamal "Embedded Systems Design", TMH. 3rd Edition 2009
2. Frank Vahid, Tony Givargis, "Embedded System Design", John Wiley. 4th Edition 2010
3. Lyla, Pearson, "Embedded Systems" 3rd Edition 2013
4. David E. Simon, "An Embedded Software Primer" Pearson Education, 4th Edition 2010

SEMESTER- I

Advanced Microprocessor for Embedded system Design

Subject Code: 14MTES102 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

Unit I

Introduction **6 Hours**

Motivation for advanced microcontrollers- Low Power embedded systems, On-chip peripherals, and low-power RF capabilities. Examples of applications.

Unit II **12 Hours**

PIC microcontroller - 8-bit Microcontroller family, PIC18 features and block diagram - PIC18 Architecture and assembly language Programming, SFRs, RISC architecture in the PIC, Branch, Call, Time delay loop, PIC I/O Port programming, addressing modes, Interrupts and Interrupt Servicing mechanisms. Peripherals: Introduction to timers, counters, watchdog timers and Real time clocks, PIC18 timer programming in assembly and C, Introduction to UART, PIC18 Serial Port programming in assembly and C.

Unit III

PIC Interfacing **06 Hours**

Introduction to Pulse width modulators, controlling a DC motor using PWM, LCD controllers and its interfacing to PIC, Keypad controllers interfacing to PIC, stepper motor controllers interfacing to PIC, ADC, DAC interfacing.

Part B

Unit IV **18 Hours**

MSP430 – 16-bit Microcontroller family, CPU architecture, Instruction set, Interrupt mechanism, Clock systems, Memory subsystem, bus-architecture. The assembly language and C programming for MSP-430 microcontrollers. On-chip peripherals- WDT, Comparator, Op-Amp, Timer, Basic Timer, Real Time clock, (RTC), ADC, DAC, Digital I/O. Using the low power modes, Clock request feature, Low – power programming and interrupts. Applications – Wireless Sensor Networking with MSP430 and Low-Power RF circuits; Pulse Width Modulation (PWM) in Power Supplies.

Unit V **18 Hours**

ARM Cortex M3

ARM -32 bit Microcontroller family. Architecture of ARM Cortex M3- General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register, Nested Vector Interrupt Controller, Interrupt behavior if ARM Cortex M3, Exceptions Programming, Advanced Programming Features, Memory Protection, Debug Architecture.

1. Muhammad Ali Mazidi, Roind D. Mckinay, Danny Causey "PIC Microcontroller and Embedded Systems using assembly and C for PIC18" Pearson Education. 3rh Edition 2009.
2. John Peatman "Design with PIC microcontroller" Printice Hall 4th Edition 2010.
3. John Davies, "MSP430 Microcontroller Basics", Newnes (Elsevier Science), 3rh Edition 2008.
4. Joseph Yiu "The Definitive Guide to the ARM Cortex,-M3", Newnes, (Elsevier), 3rh Edition 2008.

Semester –I

Embedded C

Subject Code: 14MTES103 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

Unit - I: **7 Hours**

Programming Embedded Systems in C

Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

UNIT – II: **7 Hours**

Introducing the 8051 Microcontroller Family

Introduction, The external interface of the Standard 8051, Reset requirements, Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface,Power consumption ,Conclusions

UNIT – III: **7 Hours**

Introduction to Keil software

Introduction, Installing the Keil software and loading the project, Configuring the simulator, Building the target, Running the simulation, Dissecting the program, Aside: Building the hardware, Conclusions

UNIT – IV: **8 Hours**

Reading Switches

Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic

version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

Part B

UNIT – V: **8 Hours**

Adding Structure to the Code

Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT – VI: **8 Hours**

Meeting Real-Time Constraints

Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT – VII: **8 Hours**

Operating System

Introduction, The basis of a simple embedded OS, Introducing sEOs, Using Timer 0 and Timer 1, Alternative system architectures, Important design considerations when using sEOs, Example: Milk pasteurization, Conclusions

UNIT – VIII: **7 Hours**

Case Study: Intruder Alarm System

Introduction, The software architecture, Key software components used in this example, Running the program, The software, Conclusions

REFERENCE BOOKS:

1. Michael J. Pont, "Embedded C" - Pearson Education, 2008 2nd Edition 2008.

2. Nigel Gardner "PICmicro MCU C-An introduction to programming, The Microchip PIC in CCS C" - 3rd Edition 2009.

SEMESTER –I

Embedded Real Time Operating Systems

Subject Code: 14MTES104 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

Unit I:

Introduction to Real-Time Embedded Systems and System Resources 12 Hours

Introduction to Real- Time Embedded Systems: Brief history of Real Time Systems, A brief history of embedded Systems

System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts, preemptive Fixed Priority Scheduling Polices, Real-Time OS, Thread Safe Reentrant functions.

Unit II:

Processing, I/O Resources and Memory 12 Hours

Processing: Preemptive Fixed – Priority Policy, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline-Monotonic Policy, Dynamic priority policies.

I/O Resources: Worst – Case Execution time, Intermediate I/O, Execution efficiency,

I/O Architecture. Memory: Physical hierarchy, Capacity and allocation, shared Memory, ECC Memory, Flash file systems.

Unit III:

Multi-resource Services and Soft Real-Time Services 12 Hours

Multi-resource Services:

Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.

Soft Real-Time Services: Missed Deadlines, QoS, Alternatives to rate monotonic policy, mixed hard and soft real-time services. Embedded system components:

Part B

Unit IV:

Firmware components and Debugging Components 12 Hours

Firmware components, RTOS System software mechanisms, Software application components. Debugging Components: Exceptions assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self test and diagnostics, External test equipment, Application-level debugging

Unit V:

Performance Tuning , High availability and Reliability design: 12 Hours

Performance Tuning: Basic concepts of drill-down tuning, hardware-supported profiling and tracing, Building performance monitoring into software, Path length, Efficiency, and call frequency, fundamental optimizations.

High availability and Reliability design: Reliability and Availability, Similarities and differences, Reliability, Reliable software, available software, Design trade offs, Hierarchical applications for Fail-safe design. Design of RTOS –PIC microcontroller, (Chap 13 of Book Myke Predko)

Reference Books:

1. Sam Siewert, Cengage "Real – Time Embedded Systems and Components", Learning India 2nd Edition, 2009.
2. Myke Predko, "Programming and Customizing, the PIC microcontroller", TMH, 3rd Edition, 2008.
3. Jhon Wiley, "Programming for Embedded Systems", Dreamtech Software Team, India Pvt. Ltd., 2008. 3rd Edition 2008.

SEMESTER –I

Automotive Electronics

Subject Code: 14MTES105 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

Unit I:

Automotive Fundamentals Overview – Four Stroke Cycle, Engine Control, Ignition system, Spark plug, Spark pulse generation, Ignition Timing, Drive Train, Transmission, Brakes, Steering System, Battery, Starting System. **06 Hours**

Unit II : **Sensor and actuators-** Oxygen (02/EGO) Sensors, Throttle Position Sensor (TPS), Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Ignition Timing Sensor, Hall effect Position Sensor, Shielded Field sensor, Optical Crankshaft Position Sensor, Manifold Absolute Pressure (MAP) Sensor, Strain gauge Air Temperature (AIT) Sensor, Knock Sensor, Airflow rate sensor, Throttle angle sensor. Actuators- Fuel Metering Actuator, Fuel Injector, Ignition Actuator – Exhaust After - Treatment systems - AIR Catalytic Converter, Exhaust Gas Recirculation (EGR) Evaporative Emission Systems.

12 Hours

Unit III:

Electronic Engine Control – Engine parameters, variables, Engine Performance terms, Air/Fuel Systems – Fuel Handling, Air Intake system, Air/Fuel Management – Electronic Fuel Control System, Electronic Ignition control, Idle speed control, EGR Control. **06 Hours**

Unit IV:

Automotive network architecture for ECU communications – LIN CAN, MOST and FlexRay – Intro to wireless technology for vehicle safety and driver assistance related applications - Data security in wireless communications. **06 Hours**

Part B

Unit V:

Vehicle Motion Control – Cruise Control, Chassis, Power Brakes, Antilock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, Electronically controlled suspension. **06 Hours**

Unit VI:

Drive by wire technology – throttle – by-wire and steer-by-wire systems – Drive-by-wire system benefits and performance state-of-the-art solutions.Automotive Instrumentation – Sampling, Measurement & Signal Conversion of various parameters. **06 Hours**

Unit VII:

Automotive Diagnostics – Timing Light, Engine Analyzer, On-board diagnostics, Off-board diagnostics Expert systems. Integrated Body–Interior Safety, Lighting, Entertainment Systems, Climate Control systems, Electronic HVAC Systems, Safety Systems –SIR **06 Hours**

Unit VIII:

Future Automotive Electronic Systems - Alternative Fuel Engines, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Radio navigation, Advance Driver Information System. **06 Hours**

Reference Books:-

1. William B. Ribbens: "Understanding Automotive Electronics", SAMS/Elsevier Publishing, 6th Edition.
2. Robert Bosh GmbH: "Automotive Electronics Automotive Electronics Systems and Components", John Wiley & Sons Ltd., 5th edition, 2007.

SEMESTER –I

Advanced Microprocessor Lab

Subject Code: 14MTES116 **IA Marks: 50**
Credits: 02 **Exam Marks: 50**
Hrs/week: 02 **Total Hrs: 30**

At least ten experiments are to be performed related to the subjects in 1st semester Subject code14MTES102 "Advanced Microprocessor for Embedded system Design"

SEMESTER-II

SEMESTER –II

DSP System & Architecture

Subject Code: 14MTES201 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

Unit I:

Introduction to Digital Signal Processing

Introduction, A Digital Signal-Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation. **08 Hours**

Unit II: Architectures for Programmable Digital Signal Processors

Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Features for External Interfacing. **10 Hours**

Unit III:

Programmable Digital Signal Processors

Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54xx., Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and Programming, On-Chip peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor. **10 Hours**

Unit IV:

Implementation of Basic DSP Algorithms

Introduction, The Q-notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters. **06 Hours**

Part B

Unit V:

Implementation of FFT Algorithms

Introduction, an FFT Algorithm for DFT Computation, Overflow and Scaling, Bit-Reversed Index Generation & Implementation on the TMS32OC54xx. **06 Hours**

Unit VI:

Interfacing Memory and I/O Peripherals to Programmable DSP Devices

Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA).

06 Hours

Unit VII:

Interfacing and Applications of DSP Processor

Introduction, synchronous serial interface, A CODEC interface circuit. DSP based Biotelemetry receiver, a speech processing system, an image processing system. **06 Hours**

Unit VIII:

Real-Time DSP Applications

Sinewave generators, noise generators, DTMF Tone detection, adaptive echo cancellation, acoustic echo cancellation, speech enhancement techniques. **08 Hours**

Reference Books:

1. **Avatar Singh and S. Srinivasan**, "Digital Signal Processing", Thomson Learning, 3rd edition 2008.
2. **Sen M Kuo and Bob H Lee,** "Real-Time Digital signal processing" John Wiley and Sons publications 4th edition 2009.
3. **Ifeachor E. C., Jervis B. W,** "Digital Signal Processing: A practical approach, Pearson-Education, PHI 2nd edition 2002
4. **B Venkataramani and M Bhaskar**, "Digital Signal Processors", TMH, 2nd edition 2002
5. **Peter Pirsch,** "Architectures for Digital Signal Processing", John Weily, 3rd edition 2007

SEMESTER –II

VLSI Technology and Design

Subject Code: 14MTES202 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

UNIT –I: **9 Hours**

Introduction to MOSFETs: MOS Transistor Theory – Introduction MOS Device, Fabrication and Modeling, Body Effect, Noise Margin; Latch-up.

UNIT –II: **9 Hours**

MOS Inverter : MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, Design Equations, Static Load MOS Inverters, Transistor Sizing, Static and Switching Characteristics; MOS Capacitor; Resistivity of **V**arious Layers.

UNIT –III: **8 Hours**

Symbolic and Physical Layout Systems

MOS Layers Stick/Layout Diagrams; Layout Design Rules, Issues of Scaling, Scaling factor for device parameters.

UNIT –IV: **8 Hours**

Combinational MOS Logic Circuits:

Pass Transistors/Transmission Gates; Designing with transmission gates, Primitive Logic Gates; Complex Logic Circuits.

Part B

UNIT –V: **8 Hours**

Sequential MOS Logic Circuits:

SR Latch, clocked Latch and flip flop circuits, CMOS D latch and edge triggered flip flop.

UNIT –VI: **9 Hours**

Dynamic Logic Circuits

Basic principle, non ideal effects, domino CMOS Logic, high performance dynamic CMOS Circuits, Clocking Issues, Two phase clocking.

UNIT –VII: **9 Hours**

CMOS Subsystem Design: Semiconductor memories, memory chip organization, RAM Cells, dynamic memory cell.

TEXT BOOKS:

1. S. M. Kang and Y. Leblebici, "*CMOS Digital Integrated Circuits: Analysis and Design"*, Third Edition, MH, 2009.
2. W. Wolf, "*Modern VLSI Design: System on Chip*, PH/Pearson", Third Edition, 2007.
3. N. Weste, K. Eshraghian and M. J. S. Smith, "*Principles of CMOS VLSI Design: A Systems Perspective"*, AW/Pearson, Second Edition (Expanded), 2008.
4. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, "*Digital Integrated Circuits: A Design Perspective"*, PH/Pearson, Second Edition, 2008.
5. D. A. Pucknell and K. Eshraghian, "*Basic VLSI Design: Systems and Circuits"*, PHI, Third Edition, 2009.
6. J. P. Uyemura, "*CMOS Logic Circuit Design"*, Kluwer, Second Edition, 2009.
7. J. P. Uyemura, "*Introduction to VLSI Circuits and System"*, Wiley, Third Edition 2002.
8. R. J. Baker, H. W. Li and D. E. Boyce, "*CMOS Circuit Design, Layout and Simulation"*, PH, Second Edition, 2007.

SEMESTER –II

Engineering Approach to Digital Design

Subject Code: 14MTES203 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

UNIT-I:

Introduction to Digital Design **4 Hours**

What is Digital, Specification and Implementation of digital design Structured and Trial-Error methods/approaches in design, Digital Computer Aided Design (CAD) tools.

UNIT-II:

Minimization and Design of Combinational Circuits **7 Hours**

Karnaugh Maps, Minimization of Sum of Products and Product of Sums,Design of minimal two-level gate networks, Design of multiple output two level gate networks, QM technique, NAND and NOR implementation of real life digital circuits Digital Circuit Characterization – Fan-in/Fan-out, Noise margin etc.. Combinational circuit design procedure, Design of Multiplexer, Decoder, Comparator, Design of large circuits using the above modules and design problems.

UNIT-III:

Hazard free Circuit Design **5 Hours**

Hazards in combinational circuits, types of hazards, hazard free realizations, essential and significance of hazards and design problems.

UNIT-IV:

State Machine Design Approach: Part-I **10 Hours**

Design of sequential modules – SR, D, T and J-K Flip-flops Flip-flop applications – Clock generation, Counters, Registers, Flip-flop conversions, Basic State machine concepts, types of state machines, traditional approaches to sequential design, FSM models analysis , state reduction: finding equivalent pairs, obtaining classes, minimal state table and completing the design,limitations of FSM, design problems.

Part B

UNIT-V:

State Machines Design Approach: Part-II **7 Hours**

ASM charts, state box, decision box, output box, relation between state diagrams and charts, state assignments, asm tables, assigned tables, representation, excitation tables, design problems using multiplexers and PLAs.

UNIT-VI:

Asynchronous Approach to Design: Part-III **8 Hours**

Difference between asynchronous and synchronous machines, modes of operation, analysis and design of asynchronous circuits, primitive table, reduction of flow tables, procedure, state assignment and transition table, completing the asynchronous design, hazard free realization of circuits using flipflops, design problems.

UNIT-VII:

Implementation Technology-1 **4 Hours**

Standard chips and programmable logic devices, PLDS, PLAs, FPGA VIRTEX-II architecture, digital computing, design of simple CPU.

UNIT-VIII:

Implementation Technology-2 **4 Hours**

Buffers, tri-state gates, transmission gates, NMOS, PMOS and CMOS logic gates, design problems, gate array approach to design.

TEXT BOOKS:

1. William I fletcher, "An engineering approach to digital design" PHI, 1st Edition 1990
2. Givone, "Digital principles and design" TMH, 3rd Edition 2003,
3. Charles.H.roth "Fundamentals of Logic Design", 4th Edition, 2004.

REFRENCES:

1. John F Wakerly, "Digital Design principles and practices", PHI, 2nd Edition 2000.
2. J.M,Sebastian smith, "Application specific integrated circuits", 2nd Edition 2000.

SEMESTER –II

EMBEDDED SYSTEMS COMMUNICATION AND NETWORKS

Subject Code: 14MTES204 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

Unit I: **8 Hours**

Introduction to Embedded system: a definition Properties of an embedded system, The significance of Moore's Law. Embedded systems and the system on silicon, Embedded systems and communications Embedded systems and security, Embedded systems and time constraints,Embedded systems and free software ,. Embedded systems and their design. An example of multimedia embedded system design. Conclusion

Unit II: **8 Hours**

RFID Technology Introduction. Automatic identification systems. The components of an RFID system . The different types of RFID systems. RF ranges. Information security. Standards in force Examples of implementations Conclusion

Unit III:

Hardware Security in Embedded Systems **7 Hours**

Introduction: Embedded systems and their security issues Security of the system and its data Secured hardware architectures for embedded systems

Unit IV: **7 Hours**

Communications Security in Embedded Systems: Introduction Communications security, Communications security in embedded systems

Part B

Unit V: **7 Hours**

Cross-Layer Adaptation for Multimedia Services in 802.11-Type Embedded Communications Systems Introduction Limits of layered structuring The XL concept 219

Unit VI: **7 Hours**

Relevance of the DTN Architecture to Mobile Ad Hoc Networks: Introduction. Mobile ad hoc networks Challenged networks. Delay-tolerant networks Relevance of DTNs to ad hoc mobile networks

Unit VII: **8 Hours**

Intelligent Interfaces and Mobile Communications Introduction Assisting the user with access to new internet services Modeling user behavior Synthesis of mobile and wireless networks References for intelligent interfaces for access to mobile networks

Unit VIII: **8 Hours**

Routing and Mobility Management in Personal Networks Introduction Personal environments. Routing in personal environments, Gateway discovery, Mobility management

TEXT BOOKS:

1. Francine Krief (Editor) “Communicating Embedded Systems: Networks Applications”, ISBN: 978-1-84821-144-5,320 pages, Wiley-ISTE, February 2010.

SEMESTER –II

MICRO ELECTRO MECHANICAL SYSTEM (Elective I)

Subject Code: 14MTES251 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

UNIT I:

INTRODUCTION TO MICROSYSTEMS **10 Hours**

Review of microelectronics manufacture and introduction to MEMS Overview of Microsystems technology. Laws of scaling. The multi disciplinary nature of MEMS. Survey of materials central to micro engineering. Applications of MEMS in various industries.

UNIT II:

MICRO MANUFACTURING TECHNIQUES **10 Hours**

Photolithography, Film deposition, Etching processes, Bulk micro machining, silicon surface micro machining, LIGA process, Rapid micro product development.

UNIT III:

MICRO SENSORS AND MICRO ACTUATORS **14 Hours**

Energy conversion and force generation, Electromagnetic Actuators, Reluctance motors, piezoelectric actuators, bi-metal-actuator Friction and wear. Transducer principles, Signal detection and signal processing, Mechanical and physical sensors, Acceleration sensor, pressure sensor, Sensor arrays.

Part B

UNIT IV:

INTRODUCTION TO MICRO / NANO FLUIDS **14 Hours**

Fundamentals of micro fluidics, Micro pump – introduction – Types – Mechanical Micro pump – Non Mechanical micro pumps, Actuating Principles, Design rules for micro pump – modeling and simulation, Verification and testing – Applications.

UNIT V:

MICROSYSTEMS DESIGN AND PACKAGING **12 Hours**

Design considerations, Mechanical Design, Process design, Realization of MEMS components using intellisuite. Micro system packaging, Packing Technologies, Assembly of Microsystems, Reliability in MEMS

TEXT BOOKS

1 Mohamed Gad – el – Hak , MEMS Handbook, CRC Press, 2nd Edition 2002

2 Rai-Choudhury P. MEMS and MOEMS Technology and Applications, PHI Learning Private Limited, 3rd Edition 2009.

REFERENCES

1 Sabrie Solomon, Sensors Handbook, Mc Graw Hill, 2nd Edition 1998

2 Marc F Madou, Fundamentals of Micro Fabrication, CRC Press, 2nd Edition, 2002

3 Francis E.H. Tay and W.O.Choong , Micro fluidics and Bio mems application, IEEE Press New York, 2nd Edition 1997.

4 Trimmer William S., Ed., "Micromechanics and MEMS", IEEE Press New York, 1997.

5 Maluf, Nadim, "An introduction to Micro electro mechanical Systems Engineering", AR Tech house, Boston 3rd Edition 2000.

SEMESTER –II

ADVANCED OPERATING SYSTEMS (ELECTIVE -I)

Subject Code: 14MTES252 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

UNIT –I:

Introduction to Operating Systems: **12 Hours**

Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System.

UNIT –II:

Introduction to UNIX and LINUX: 12 Hours

Basic commands & command arguments, Standard input, output, Input / output redirection, filters and editors, Shells and operations.

UNIT –III:

System Calls: 12 Hours

System calls and related file structures, Input / Output, Process creation & termination.

Inter Process Communication

Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

Part B

UNIT –IV: 12 Hours

Introduction to Distributed Systems:

Goals of distributed system, Hardware and software concepts, Design issues.

Communication in Distributed Systems:

Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group Communication.

UNIT –V: 12 Hours

Synchronization in Distributed Systems:

Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions

Deadlocks:

Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:

1. The design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete reference LINUX – Richard Peterson, 4th Eition., McGraw – Hill.

REFERENCE BOOKS:

1. Operating Systems: Internal and Design Principles - Stallings, 6th Edition, PE.
2. Modern Operating Systems, Andrew S Tanenbaum, 3rd Edition, PE.
3. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Edition, John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens, 2nd Edition 1998, PHI.

SEMESTER –II

SYSTEM ON CHIP ARCHITECTURE (ELECTIVE -I)

Subject Code: 14MTES253 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

UNIT –I:

Introduction to the System Approach: **12 Hours**

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT –II: **12 Hours**

Processors:

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers:

minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III: 12 Hours

Memory Design for SOC:

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

Part B

UNIT -IV: 12 Hours

Interconnect Customization and Configuration:

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V: 12 Hours

Application Studies / Case Studies:

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Edition, 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Ricardo Reis, "Design of System on a Chip: Devices and Components", Springer, 1st Edition, 2004,
2. Jason Andrews – Newnes, "Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)", BK and CDROM.
3. Prakash Rashinkar, Peter Paterson and Leena Singh L, "System on Chip Verification – Methodologies and Techniques" 2001, Kluwer Academic Publishers.

SEMESTER –II

Wireless LAN's and PAN's (ELECTIVE -I)

Subject Code: 14MTES254 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

UNIT I: Overview of Wireless Communication **7 Hours**

History of wireless communication, Wireless Vision, Technical Issues, Current Wireless Systems, The Wireless Spectrum.

Unit II: Introduction to Wireless LANS **10 Hours**

Historical Overview of LAN Industry, Evolution of The WLAN Industry, Wireless Home Networking, WLAN Application, WLAN Components, WLAN Modes, WLAN Standards and operation.

Unit III: High-speed Wireless LANs and WLAN Security **8 Hours**

IEEE 802.11a and IEEE 802.11b and other WLAN Standards, WLAN Security.

Unit IV: Low Rate Wireless Personal Area Networks **10 Hours**

Infrared WPANs, RFWPANs, Low rate WPAN Security, High rate WPAN Standards, 802.15.3, High rate WPANs, Ultra Wideband, WPAN Challenges.

Unit V: Wireless Wide Area Networks*:* **9 Hours**

Cellular Telephone Applications, Digital Cellular Technology, Client Software, Digital Cellular Challenges and Outlook, Satellite Broadband Wireless.

Part B

Unit VI: Wireless Metropolitan Area Networks*:* **8 Hours**

What is WMAN?, Land- Based Fixed Broadband Wireless, IEEE 802.16 (WiMAX), WMAN Security.

Unit VII: Ad-Hoc- Wireless Networks **10 Hours**

Application, Design Principles and Challenges, Protocol Layers, Cross Layer Design, Network Capacity Limits, Energy Constrained Networks. Cellular and Adhoc wireless networks, applications, MAC protocols, Routing, Multicasting, Transport layer Protocols, quality of service browsining, deployment considerations, Adhoc wireless Internet.

TEXT BOOKS:

1. Andrea Goldsmith, "Wireless Communication", Cambridge University Press.
2. Marks Ciampor, Jeorge Olenewa "Wireless Communication", 2007, Cengage Learning.
3. Kaveh Pahlaram, Prashant Krishnamurthy, "Wireless Networks" 2002, PHI.

SEMESTER –II

VLSI and Embedded System Design Lab

Subject Code: 14MTES216 **IA Marks: 50**
Credits: 02 **Exam Marks: 50**
Hrs./week: 02 **Total Hrs: 30**

The following programs are to be implemented on ARM based Processors and MSP430

PART- I

1. Simple Assembly Program for
   a. Addition | Subtraction | Multiplication | Division
   b. Operating Modes, System Calls and Interrupts
   c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
5. Program to demonstrates a simple interrupt handler and setting up a timer
6. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
7. Program to Interface 8 Bit LED and Switch Interface , Buzzer Interface on IDE environment
8. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
9. Program to demonstrate I2C Interface on IDE environment for Serial EEPROM
10. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
11. Program for Generation of PWM Signal
12. Program to interface ADC and DAC
13. Write an Assembly and C Programming to interface DS1306 RTC using SPI Protocol.
14. Write an Assembly and C Programming to interface Relay, DC, and Stepper Motors.

PART-II

Design the following using Cadence Virtuoso Schematic Editor and Virtuoso Layout Suite

a. Draw the schematic and verify the following

- **i. DC/AC Analysis**
- **ii. Transient Analysis**

b. Draw the Layout and verify the DRC

c. Check for LVS and Extract RC

1. Design CMOS Inverter, CMOS AND and NAND Gate, CMOS OR and NOR Gate, CMOS EX-OR and EX-NOR Gate, SR NAND Latch and SR NOR Latch.
2. Cascade Amplifier
3. Folded Cascade Amplifier.
4. Current Mirror and Cascaded Current Mirror.
5. CMOS Op-amp single Stage and Differential Amplifier
6. Common Source Amplifier, Common Drain Amplifier and Common Gate Amplifier.
7. Current Controlled Voltage source.

Semester III

SEMESTER –III

Electronic Packaging

Subject Code: 14MTES301 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

Unit I: **8 Hours**

Definition of a system and history of semiconductors, Products and levels of packaging, Packaging aspects of handheld products, Definition of PWB, Basics of Semiconductor and Process flowchart, Wafer fabrication, inspection and testing, Wafer packaging; Packaging evolution; Chip connection choices, Wire bonding, TAB and flip chip.

Unit II: **16 Hours**

Functions of an Electronic Package, Packaging Hierarchy, Driving Forces on Packaging Technology, Materials for Microelectronic packaging, Packaging Material Properties, Ceramics, Polymers, and Metals in Packaging, Material for high-density interconnect substrates, Electrical Anatomy of Systems Packaging, Signal Distribution, Power Distribution, Electromagnetic Interference, Design Process, Processing Technologies – Thin Film deposition, Patterning, Metal to Metal joining

Unit III: **12 Hours**

Design for Reliability – Fundamentals, Induced failures. IC Assembly – Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding, Flip Chip, Wafer Level Packaging. Discrete, Integrated and Embedded Passives.

Part B

Unit IV: **12 Hours**

Printed Circuit Board – Anatomy, CAD tools for PCB design, Standard fabrication, Micro via Boards. Board Assembly – Surface Mount Technology, Through-Hole Technology, and Process Control and Design challenges.

Unit V: **12 Hours**

Thermal Management for IC and PWBs, Cooling Requirements, Electronic cooling methods, Electrical Testing – System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability.

References:

1. Rao R. Tummala : "Fundamentals of Microsystem Packaging" McGraw Hill 4th Edition 2008.
2. Richard K. Ulrich &William D. Brown "Advanced Electronic Packaging" - IEEE Press. 2nd Edition 2009.

SEMESTER –III

Model Based Development of Embedded system

Subject Code: 14MTES302 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

Unit I:

Performance Analysis of Embedded Systems **6 Hours**

System-Level Performance Analysis, Application Scenario, Representation in the Time Domain, Modular Performance Analysis with Real-Time Calculus, RTC Toolbox.

Unit II:

System C and Heterogeneous Embedded Systems **10 Hours**

Introduction, Performance Analysis of Distributed Embedded Systems, Transaction-Level Modeling, Proposed Hybrid Approach for Accurate Software Timing Simulation, Formal Multiprocessor Performance Analysis, From Distributed Systems to MPSoCs, Hierarchical Communication, Scenario-Aware Analysis, Sensitivity Analysis, Robustness Optimization.

Unit III:

Model-Based Framework for Schedulability Analysis **8 Hours**

Introduction, UPPAAL and Its Formalism, Schedulability Problems, Framework Model in UPPAAL, Framework Instantiation.

Unit IV: **8 Hours**

Modeling and Analysis Framework for Embedded Systems

Introduction, Embedded Systems Model, Model of Computation, MoVES Analysis Framework, Summary.

Part B

Unit V: **8 Hours**

Model based design of MPSoCs

Introduction, MultiFlex Platform Mapping Technology Overview, MultiFlex Streaming, Mapping Flow, MultiFlex Streaming Mapping Tools.

UnitVI: **8 Hours**

Embedded Software Design Methodology for MPSoCs

Introduction, Proposed Workflow of Embedded Software Development, Common Intermediate Code, CIC Translator.

Unit VII:

Programming Models for MPSoC **10 Hours**

Introduction, Hardware–Software Architecture forMPSoC, Programming Models, Existing Programming Models, Simulink- and SystemC-Based MPSoCs Programming Environment, Experiments with H.264 Encoder Application, Design Challenge Platform-Based Design

Unit VIII: **8 Hours**

Multidomain embedded systems

Introduction, Modeling, Verification, and Testing Using Timed and Hybrid Automata, Modeling with Timed and Hybrid Automata, Exhaustive Verification, Partial Verification, testing, test Generation for Timed Automata, Test Generation for Hybrid Automata.

References:

1. **Gabriele Nicolescu** and **Peter J Mostermann**, "Model based design of embedded systems" by, CRC Press, First Edition, 2010.
2. **Raj Kamal**, "Embedded systems architecture, programming and design", Tata McGraw hill, 2nd Edition, 2010.
3. **Justyna Zander, Ina Schieferdecker,** and **Pieter J. Mosterman,** "Model-Based Testing for Embedded Systems", CRC Press.

SEMESTER –III

Hardware and Software Co-Design (ELECTIVE -II)

Subject Code: 14MTES331 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

UNIT –I: **12 Hours**

Co- Design Issues:

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms:

Hardware software synthesis algorithms: hardware – software partitioning distributed system cosynthesis.

UNIT –II: 12 Hours

Prototyping and Emulation:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III: 12 Hours

Compilation Techniques and Tools for Embedded Processor Architectures:

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

Part B

UNIT –IV: 12 Hours

Design Specification and Verification:

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V: 12 Hours

Languages for System – Level Specification and Design-I:

System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Wolf, "Hardware / Software Co- Design Principles and Practice", Springer, 2nd Edition 2009.
2. Giovanni De Micheli, Mariagiovanna Sami, Kluwer "Hardware / Software Co- Design" Academic Publishers, 2nd Edition 2002.

REFERENCE BOOKS:

1. Patrick R. Schaumont "A Practical Introduction to Hardware/Software Co-design"– Springer, 4th edition 2010.

SEMESTER –III

Embedded Computing (ELECTIVE -II)

Subject Code: 14MTES332 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

UNIT –I: **12 Hours**

Programming on Linux Platform:

System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box. **Operating System Overview**: Processes, Tasks, Threads, Multi-Threading, Semaphore, Message Queue.

UNIT –II: **12 Hours**

Introduction to Software Development Tools:

GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools.

UNIT –III: **12 Hours**

Interfacing Modules:

Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

Part B

UNIT –IV: **12 Hours**

Networking Basics:

Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.

UNIT –V: **12 Hours**

IA32 Instruction Set: application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

TEXT BOOKS:

1. Peter Barry and Patrick Crowley, "Modern Embedded Computing", Elsevier/Morgan Kaufmann, 1st Edition 2012.

2. Michael K. Johnson, Erik W. Troan, "Linux Application Development" Adission Wesley, 1998.
3. Kip R. Irvine "Assembly Language for x86 Processors"
4. "Intel® 64 and IA-32 Architectures Software Developer Manuals".

REFERENCE BOOKS:

1. Abraham Silberschatz, Peter B. Galvin and Greg Gagne “Operating System Concepts”.
2. Maurice J. “The Design of the UNIX Operating System” Bach Prentice-Hall.
3. W. Richard Stevens “UNIX Network Programming”.

Semester-III

Advanced Computer Architecture (Elective II)

Subject Code: 14MTES333 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

UNIT-I: **06 Hours**

Parallel Computer Models The State of Computing, Multiprocessors and Multicomputer, Multivector and SIMD Computers.

UNIT-II: **10 Hours**

Processors and Memory Hierarchy, Advanced Processor Technology, Superscalar and Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology.

UNIT-III: **08 Hours**

Bus, Cache, and Shared Memory Backplane Bus Systems, Cache Memory Organizations, Shared Memory Organization.

UNIT-IV: **08 Hours**

Pipelining and Superscalar Techniques, Linear pipeline Processors, Nonlinear Pipeline Processors, Instruction Pipeline Design, Arithmetic Pipeline Design, Super Scalar and Super Pipeline Design.

Part B

UNIT-V: **10 Hours**

Multiprocessors and Multicomputer, Multiprocessors System Interconnects, The Cache coherence and Synchronization Mechanism, Three Generations of Multicomputer, Message–Passing Mechanisms,

UNIT-VI: **10 Hours**

Scalable, Multithreaded, and Dataflow Architectures, Latency-Hiding Techniques, Principles of Multithreading, Fine-Grain Multicomputer, Scalable and Multithread Architecture, Data flow and Hybrid Architectures.

UNIT-VII: **08 Hours**

UNIX, Mach, and OSF/1 for Parallel Computers, Multiprocessor UNIX Design Goals, Master – Slave and Multithread UNIX, Multicomputer UNIX Extensions, Mach/OS Kernel Architecture and applications.

Text Book:

Kai Hwang, "Advanced Computer Architecture- Parallelism, Scalability, Programmability" Printice Hall 4th Edition 2010.

Reference Books:

Hennssey & Petterson "Computer Architecture A Quantitative Approach". Pearson Education 3rd Edition 2009

Semester –III
CRYPTOGRAPHY AND NETWORK SECURITY (Elective II)

Subject Code: 14MTES334 **IA Marks: 50**
Credits: 04 **Exam Marks: 50**
Hrs/week: 04 **Total hrs: 60**

Part A

UNIT-I:

Introduction **6 Hours**

Services, Mechanisms and attacks, OSI security architecture, Model for network security. **Classical Encryption Techniques:** Symmetric cipher model, Substitution techniques, Transposition techniques, Rotor machine, Steganography, Problems.

UNIT-II:

Block Ciphers and Data Encryption Standard **8 Hours**

Block cipher principles, the data encryption standard, DES, Strength of DES, Block cipher design principles, Block cipher modes of operation, Problems.

UNIT-III:

Public Key Cryptography and RSA **10 Hours**

Principles of public key cryptosystems, RSA algorithm, Problems. Key Management and other Public Key Cryptosystems- Key management, Diffie-Hellman key exchange, Problems. Elliptic curve arithmetic, Elliptic curve cryptography.

UNIT-IV:

Message Authentication and Hash Functions **7 Hours**

Authentication requirements, Authentication functions, Message authentication codes, Hash functions, Security of hash functions and MAC's, Problems.

Part B

UNIT-V:

Digital Signature and Authentication Protocol **7 Hours**

Digital signature, Authentication protocols, Digital signature standard.

UNIT-VI:

Authentication Applications **10 Hours**

Kerberos, X.509 authentication service, Problems, Public key infrastructure.

Firewalls: Firewall design principles; Trusted systems, Problems.

UNIT-VII:

Electronic Mail Security **and** ***IP Security*** **12 Hours**

Pretty good privacy, S/MIME, Data compression using ZIP, Radix-64 conversion, PGP random number generation. IP security overview, IP security architecture, Authentication header, Encapsulating security pay load, combining security associations, Key management, Problems.

Reference Books:

1. William Stallings, "Cryptography and Network Security", Pearson Education (Asia) Pvt. Ltd., 4th edition, 2009.
2. C. Kaufman, R. Perlman, and M. Speciner, "Network Security: Private Communication in a Public World", 2nd edition, Pearson Education (Asia) Pvt. Ltd., 2nd edition, 2002.
3. Atul Kahate, "Cryptography and Network Security", Tata McGraw-Hill, 2nd edition, 2003.
4. Eric Maiwald, "Fundamentals of Network Security", McGraw- Hill, 2nd edition, 2003.

SEMESTER –IV

PROJECT WORK